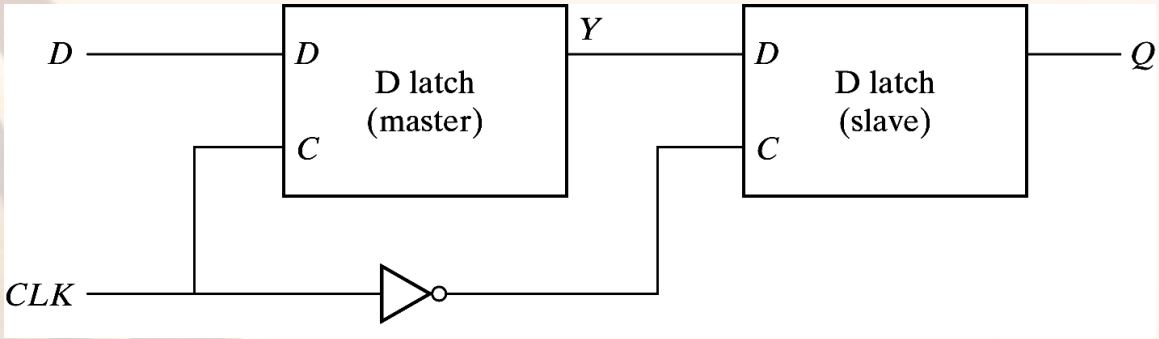
Lecture 8

Synchronous Sequential Logic continue

Outline

- Flip Flops
- Analysis of Clocked Sequential Circuits
- Design Procedure

Master-Slave D Flip-Flop



- Constructed with two D latches and an inverter
- The first latch (master) is enabled when CLK=1
  - It reads the input changes but stops before the second one
- The second latch (slave) is enabled when CLK=0
  - Close the first latch to isolate the input changes
  - Deliver the final value at the moment just before CLK changes
- The circuit samples the D input and changes its output Q only at the **negative-edge of the controlling clock**

Edge-Triggered D Flip-Flop

- If only SR latches are available, three latches are required
- Two latches are used for locking the two inputs (CLK & D)
- The final latch provides the output of the flip-flop

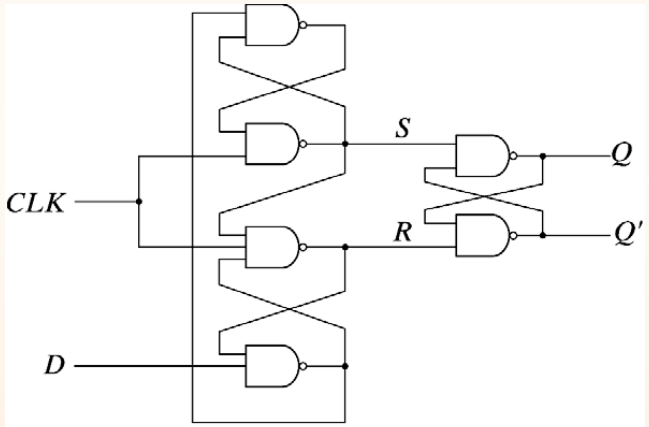
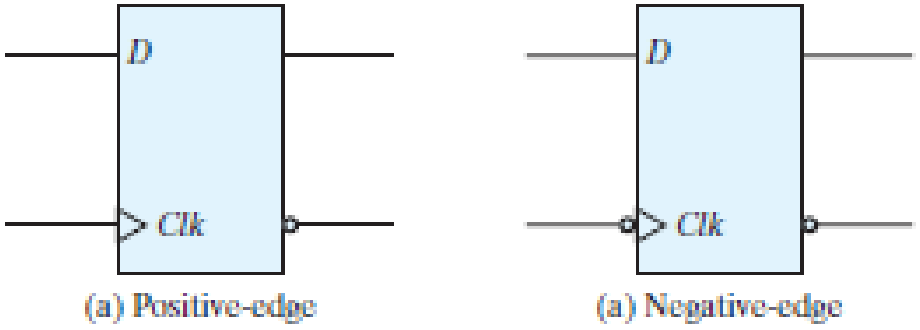


Fig. 5-10 *D*-Type Positive-Edge-Triggered Flip-Flop



Graphic symbol for edge-triggered *D flip-flop*

Setup & Hold Times

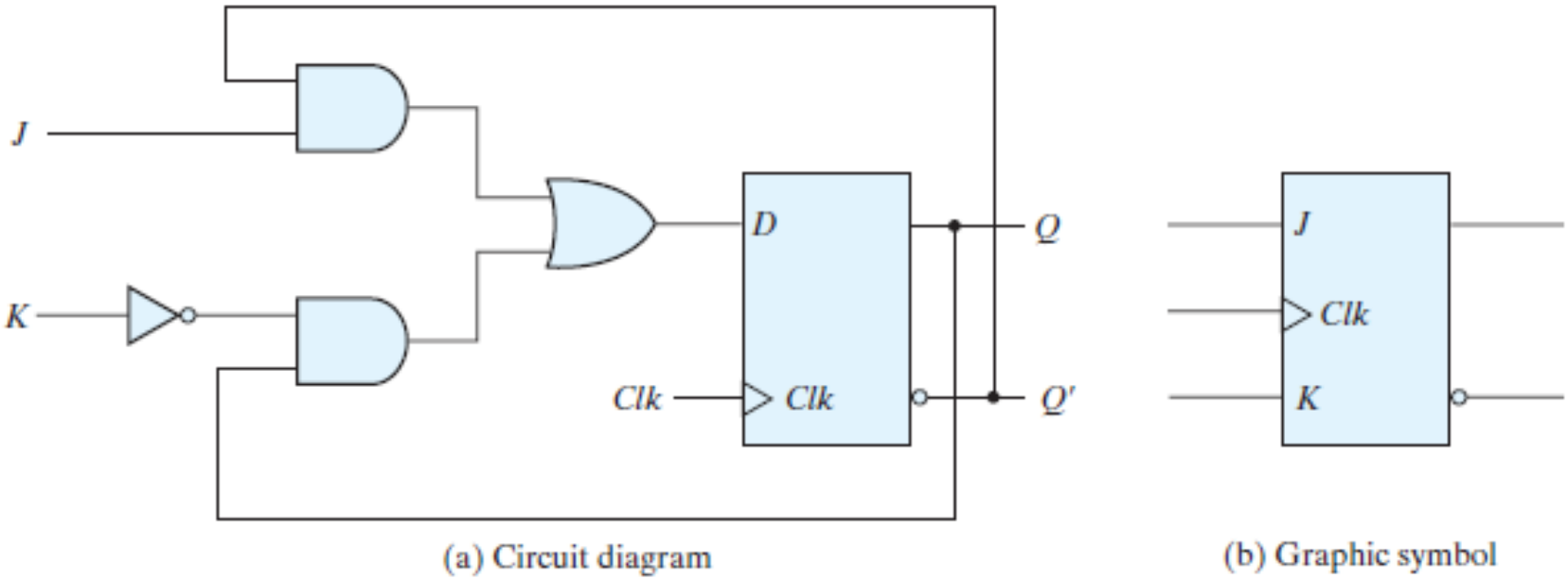
- The response time of a flip-flop to input changes must be taken into consideration
- Setup Time: The length of time that data must stabilize before the clock transition
  - The maximum data path is used to determine if the setup time is met
- Hold Time: The length of time that data must remain stable at the input pin after the active clock transition
  - The minimum data path is used to determine if hold time is met

Other Flip-Flops

- The most economical and efficient flip-flop is the edge-triggered D flip-flop
  - It requires the smallest number of gates
- Other types of flip-flops can be constructed by using the D flip-flop and external logic
  - JK flip-flop
  - T flip-flops
- Three major operations that can be performed with a flip-flop:
  - Set it to 1
  - Reset it to 0
  - Complement its output

Edge-Triggered JK Flip-Flop

$$D = JQ' + K'Q$$

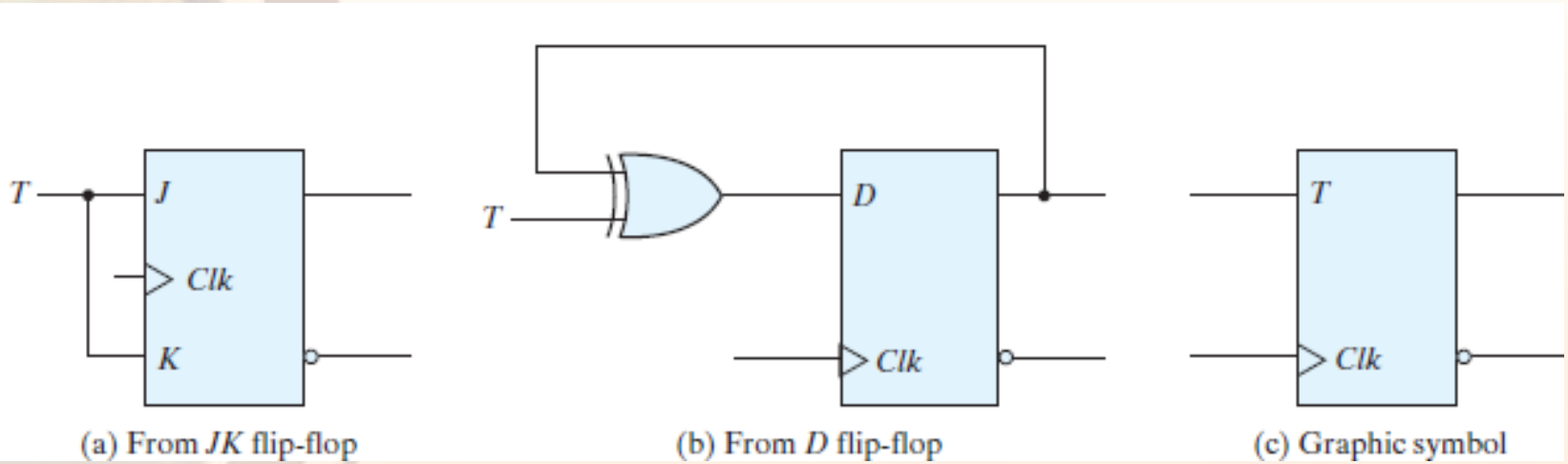


(a) Circuit diagram (b) Graphic symbol

FIGURE 5.12: ***JK flip-flop***

Edge-Triggered T Flip-Flop

$$D = T \oplus Q = TQ' + T'Q$$



(a) From *JK* flip-flop (b) From *D* flip-flop (c) Graphic symbol

FIGURE 5.13: ***T flip-flop***

T=0: hold
T=1: toggle

Characteristic Tables

- Define the logical properties in tabular form

D Flip-Flop

D	Q(t + 1)	
0	0	Reset
1	1	Set

JK Flip-Flop

J	K	Q(t + 1)	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement

T Flip-Flop

T	Q(t + 1)	
0	$Q(t)$	No change
1	$Q'(t)$	Complement

Characteristic Equations

- Algebraically describe the next state
- Can be derived from characteristic tables

- D flip-flop:

  $Q(t+1) = D$

- JK flip-flop:

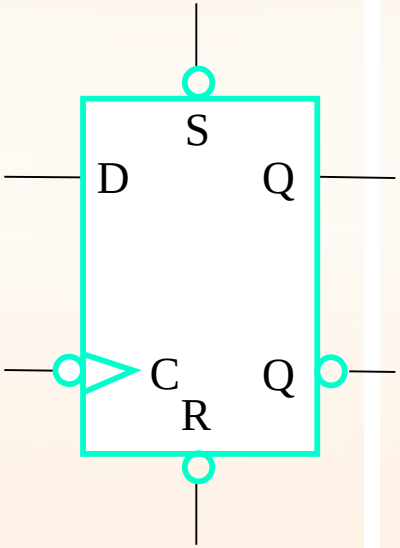
  $Q(t+1) = JQ' + K'Q$

- T flip-flop:

  $Q(t+1) = T \oplus Q = TQ' + T'Q$

Direct Inputs

- Force the flip-flop to a particular state immediately
  - Independent of clock signal
  - Have higher priority than any other inputs
  - Useful to bring all flip-flops from unknown into known state while power up
- The input that sets the flip-flop to 1 is called **preset or direct set**
- The input that clears the flip-flop to 0 is called **clear or direct reset**
- Also called **asynchronous set/reset**



Sequential Circuit Analysis

- The behavior of a clocked sequential circuit is determined from
  - The inputs
  - The outputs
  - The state of its flip-flops
- The outputs and the next state are both a function of the inputs and the present state
- To analyze a sequential circuit, we can use
  - State equations
  - State table
  - State diagram
  - Flip-Flop input equations

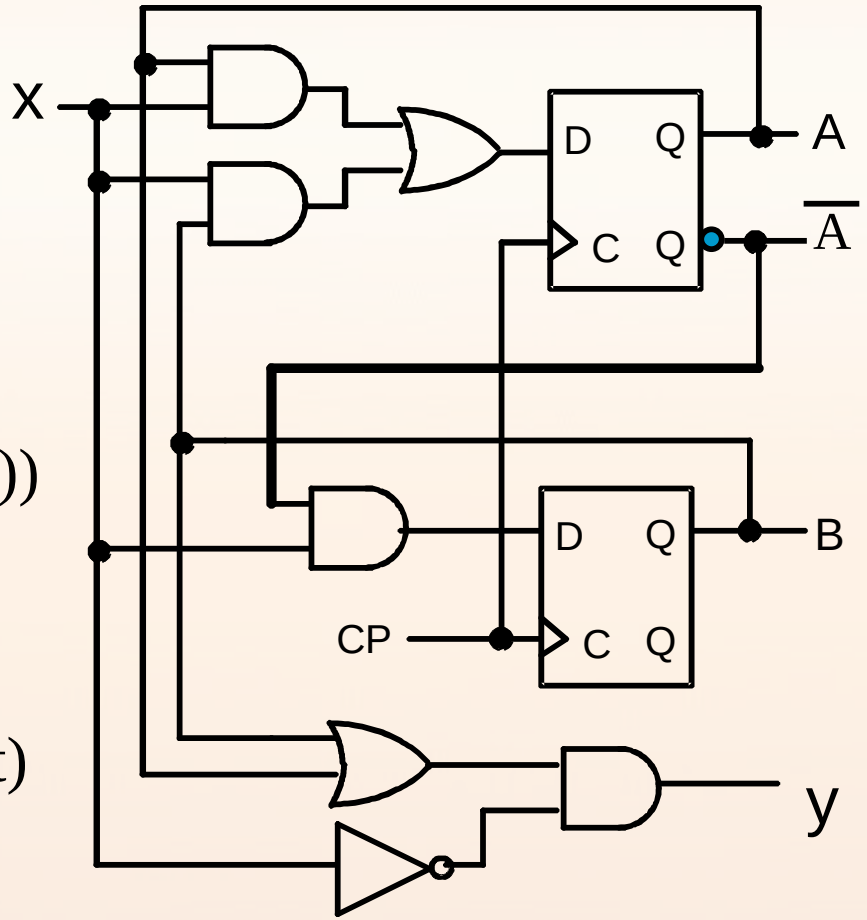
State Equations

- Input: x(t)
- Output: y(t)
- State: (A(t), B(t))
- What is the Output Function?

$$y(t) = \overline{x}(t)(B(t) + A(t))$$

- What is the Next State Function?

$$A(t+1) = A(t)x(t) + B(t)x(t)$$
$$B(t+1) = \overline{A}(t)x(t)$$



State Table(transition table)

- Enumerate the time sequence of inputs, outputs, and flip-flop states
  - Also called transition table
  - Similar to list the truth table of state equations
- Consist of four sections
  - Present state, input, next state, and output
- A sequential circuit with m flip-flops and n inputs need 2^{m+n} rows in the state table

Present state		input	Next state		output
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

Second Form of State Table

- The state table has only three section: present state, next state, and output
- The input conditions are enumerated under next state and output sections

Present State	Next State		Output	
	x(t)=0	x(t)=1	x(t)=0	x(t)=1
A(t) B(t)	A(t+1)B(t+1)	A(t+1)B(t+1)	y(t)	y(t)
0 0	0 0	0 1	0	0
0 1	0 0	1 1	1	0
1 0	0 0	1 0	1	0
1 1	0 0	1 0	1	0

State Diagram

- Graphically represent the information in a state table
  - Circle: a state (with its state value inside)
  - Directed lines: state transitions (with inputs/outputs above)

- Ex: starting from state 00
- If the input is 0, it stays at state 00 with output=0
- If the input is 1, it goes to state 01 with output=0
- The state table is easier to derive from a given logic diagram and state equations
- The state diagram is suitable for human interpretation

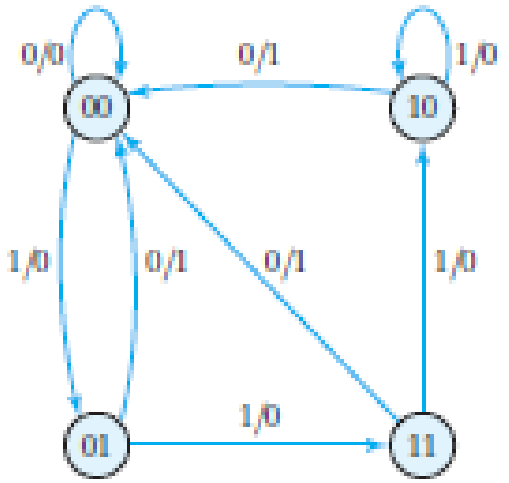


FIGURE 5.16
State diagram of the circuit of Fig. 5.15

Flip-Flop Input Equations

- To draw the logic diagram of a sequential circuit, we need
  - The type of flip-flops
  - A list of Boolean expressions of the combinational circuits
- The Boolean functions for the circuit that generates external outputs is called output equations
- The Boolean functions for the circuit that generates the inputs to flip-flops is flip-flop input equations
- Sometimes called excitation equations
- The flip-flop input equations provide a convenient form for specifying the logic diagram of a sequential circuit
- Ex: (Fig. 5-15)

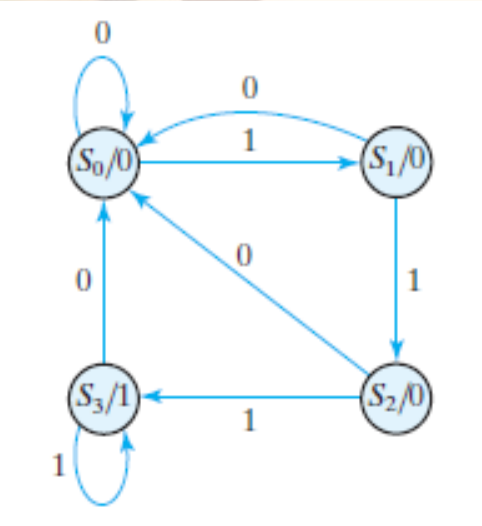
Input:	Output:
$DA=Ax+Bx$	$y=(A+B)x'$
$DB=A'x$	

Design Procedure

- Design procedure of synchronous sequential circuits:
  1. Derive a state diagram for the circuit from specifications
  2. Reduce the number of states if necessary
  3. Assign binary values to the states
  4. Obtain the binary-coded state table
  5. Choose the type of flip-flop to be used
  6. Derive the simplified flip-flop input equations and output equations
  7. Draw the logic diagram
- Step 4 to 7 can be automated
  - Use HDL synthesis tools

Synthesis Using D Flip-Flops

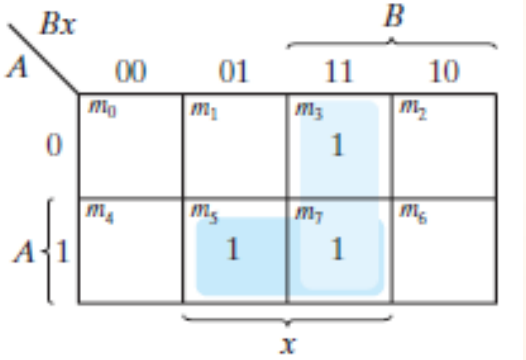
- Ex: design a circuit that detects a sequence of three or more consecutive 1's in a string of bits coming through an input line

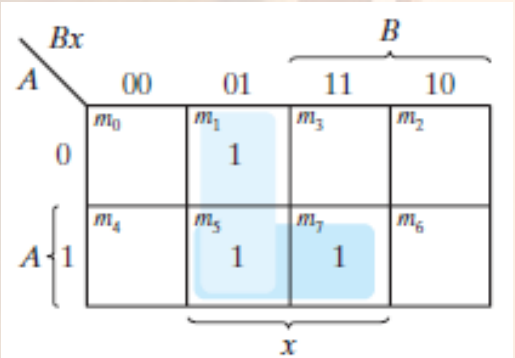


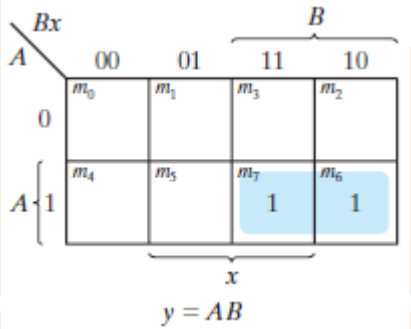
Present state		Input	Next state		Output
A	B	X	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	1	1	1	1

$$A(t+1) = D_A(A,B,x) = \sum(3,5,7)$$
$$B(t+1) = D_B(A,B,x) = \sum(1,5,7)$$
$$y(A,B,x) = \sum(6,7)$$

Synthesis Using D Flip-Flops







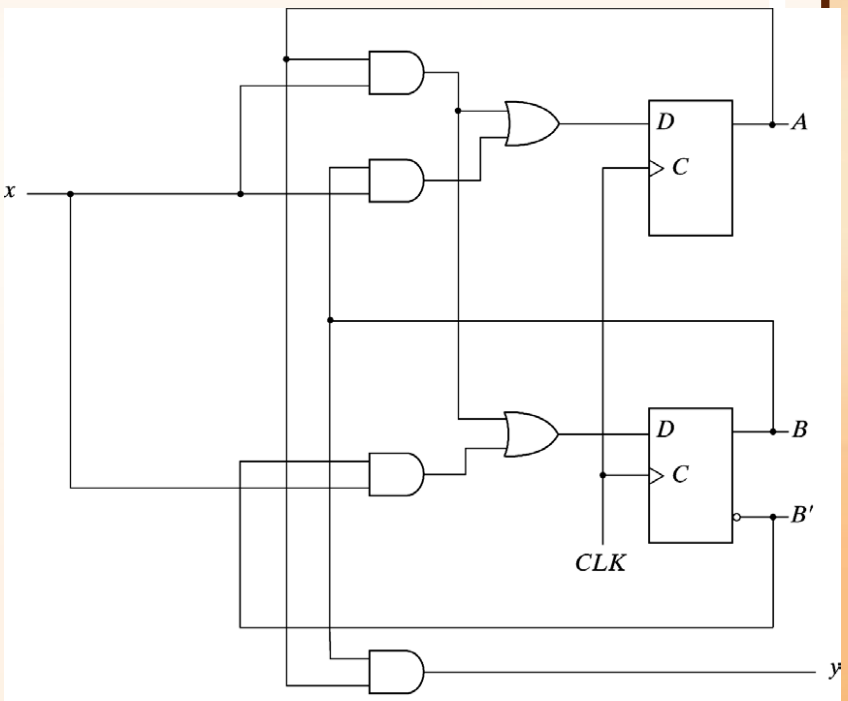


Fig. 5-26 Logic Diagram of Sequence Detector

Excitation Tables

- Record the flip-flop input conditions that will cause the required transition in STG
  - Equal to next state equations for D flip-flop
- For JK flip-flop:
  - J=0, K=X: no change (JK=00) or set to zero (JK=01)
  - J=1, K=X: toggle (JK=11) or set to one (JK=10)
  - J=X, K=1: toggle (JK=11) or set to zero (JK=01)
  - J=X, K=0: no change (JK=00) or set to one (JK=10)

JK F/F

Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Q(t)	Q(t+1)	T
0	0	0
0	1	1
1	0	1
1	1	0

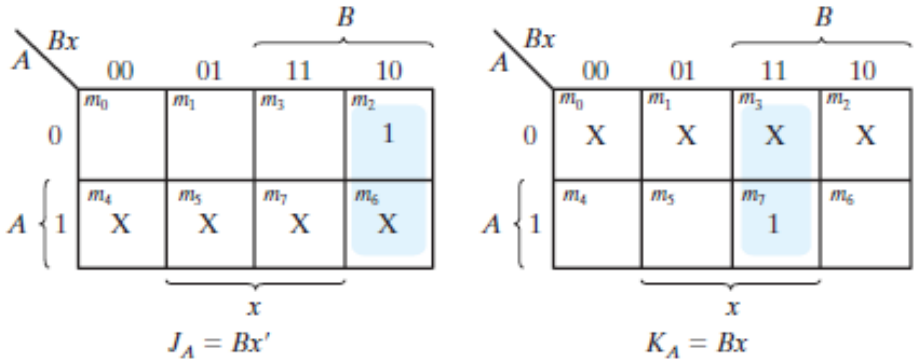
T F/F

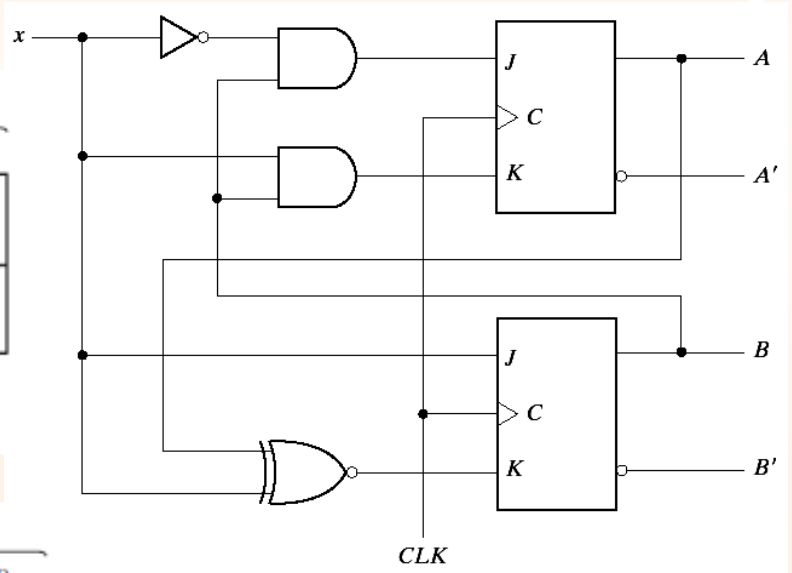
Synthesis Using JK Flip-Flops

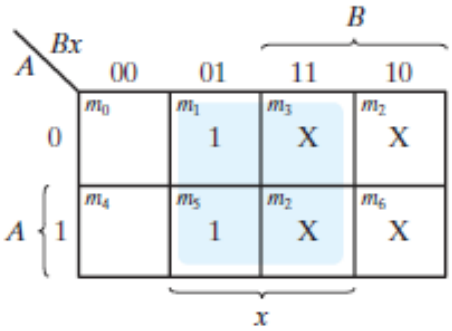
- Derive the state table with the excitation inputs

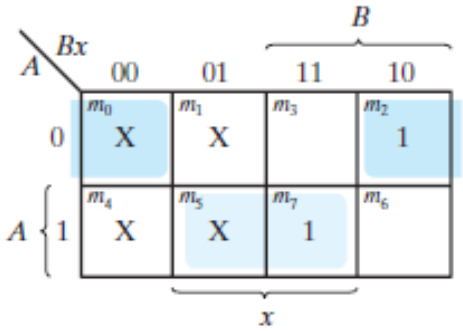
Present State		Input	Next State		Flip-Flop Inputs			
A	B	X	A	B	J_A	K_A	J_B	K_B
0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	X	1	X
0	1	0	1	0	1	X	X	1
0	1	1	0	1	0	X	X	0
1	0	0	1	0	X	0	0	X
1	0	1	1	1	X	0	1	X
1	1	0	1	1	X	0	X	0
1	1	1	0	0	X	1	X	1

Synthesis Using JK Flip-Flops



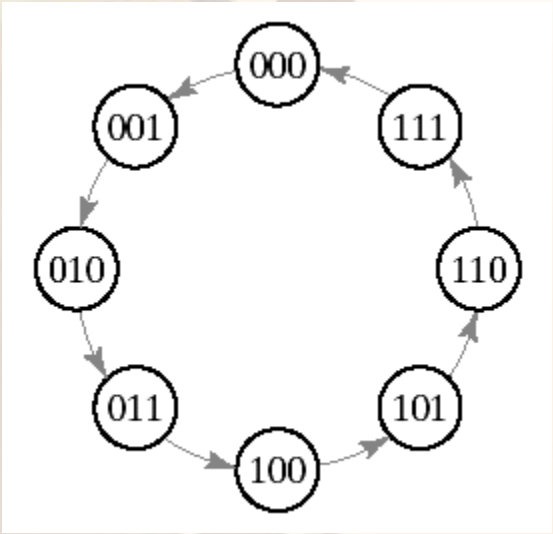






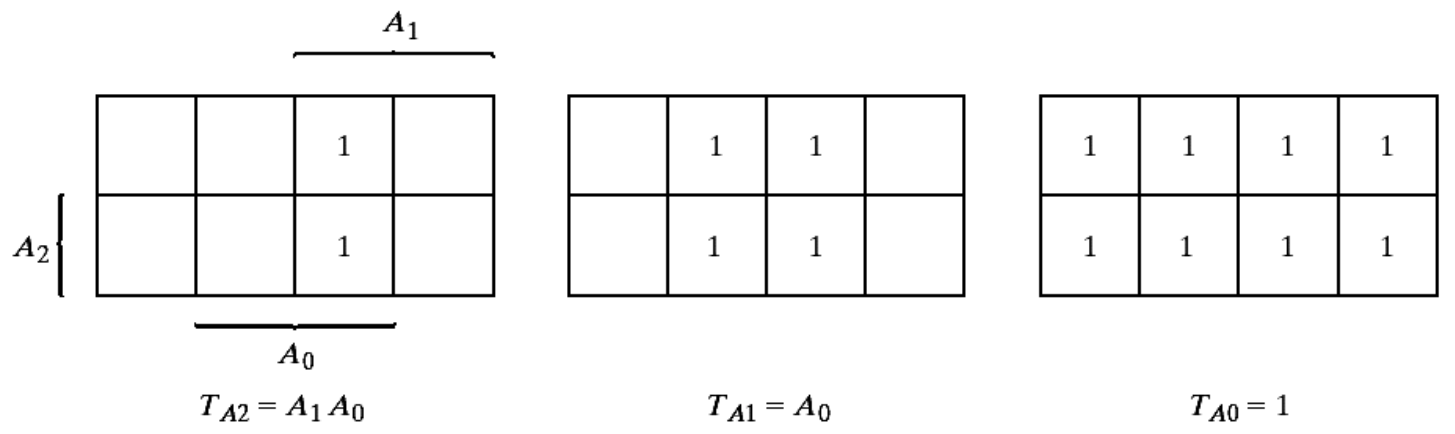
Synthesis using T Flip-Flop

- 3-bit binary counter



Present State			Next State			Flip-Flop Inputs		
A2	A1	A0	A2	A1	A0	T_{A2}	T_{A1}	T_{A0}
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

T flip-Flop for 3-bit binary counter



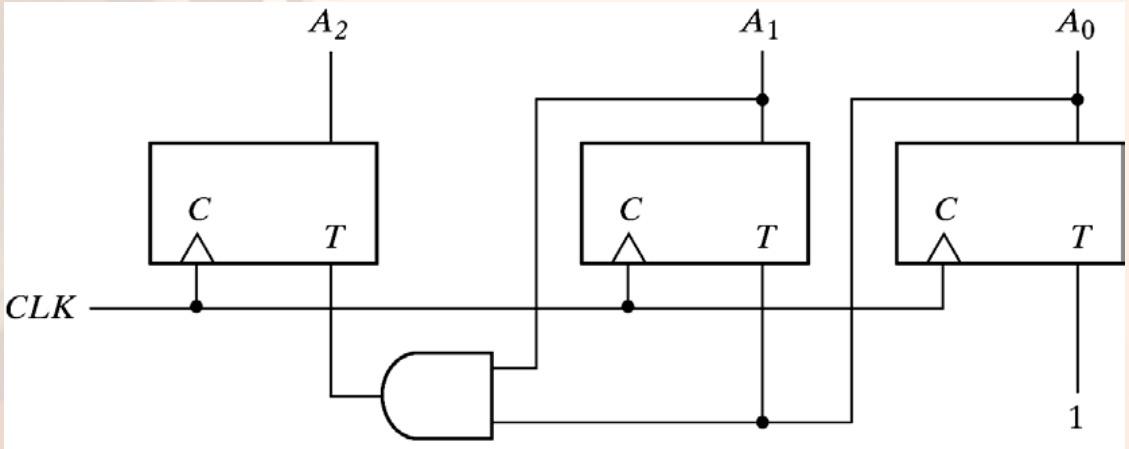


FIGURE 5.34:Logic diagram of three-bit binary counter

Home work 1

- A sequential circuit has one flip-flop *Q, two inputs x and y, and one output S . It consists* of a full-adder circuit connected to a *D flip-flop, as shown in Fig. P5.7 . Derive the state* table and state diagram of the sequential circuit.

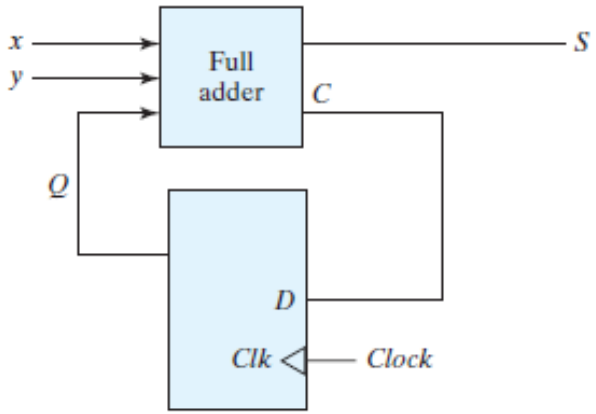


FIGURE P5.7

Home work 2

Design a sequential circuit with two *D flip-flops A and B, and one input x* .When *x = 0, the state of the circuit remains the same. When x = 1, the circuit* goes through the state transitions from 00 to 01, to 11, to 10, back to 00, and repeats.

Home work 3

Design a sequential circuit with two *JK flip-flops A and B and two inputs E and F . If E = 0,* the circuit remains in the same state regardless of the value of *F. When E = 1 and F = 1, the* circuit goes through the state transitions from 00 to 01, to 10, to 11, back to 00, and repeats. When *E = 1 and F = 0, the circuit goes through the state transitions from 00 to 11, to 10, to* 01, back to 00, and repeats

reading

- M. Morris Mano , Michael D. Ciletti “Digital Design With an Introduction to the Verilog HDL” FIFTH EDITION
  - Sections: 5.4 ,5.5(pages 198-214)